In the claims:

Claims 1 - 8 (Canceled).

9. (Original) An edge seal around the periphery of an integrated circuit device comprising:

a. a semiconductor substrate;

b. a layer of dielectric material over the semiconductor substrate, the layer of dielectric material comprising a low-k dielectric material;

c. a metallic wall of a high conductivity metal in the layer of dielectric material; and

d. a layer of insulation material between the metallic wall and the dielectric material, wherein the insulation material and dielectric material are different materials.

10. (Original) The edge seal of claim 9 wherein the low-k dielectric material comprises SiLK or fluoridized polyimide.

11. (Original) The edge seal of claim 9 wherein the layer of dielectric material comprises a bottom layer on the semiconductor substrate, the low-k dielectric material on the bottom layer and a top moisture barrier on the low-k dielectric material.

12. (Original) The edge seal of claim 9 wherein the insulation material is selected from the group consisting of SiO_2, SiC, Si_3N4, Al_2O_3, diamond like carbon, polyimide and combinations thereof.

13. (Original) The edge seal of claim 9 further comprising a barrier layer between the metallic wall and the insulation material wherein the barrier layer is selected from the group consisting of tantalum, tantalum nitride, chromium/ chromium oxide, titanium, titanium nitride, tungsten silicide and combinations thereof.

14. (Original) The edge seal of claim 9 wherein the high conductivity metal is copper.

15. (Original) The edge seal of claim 9 wherein the thickness of the insulation material is 0.05 microns to 0.5 microns.

16. (Original) The edge seal of claim 9 wherein there are two metallic walls in the at least one layer of dielectric material and there is a layer of insulation material between the dielectric material and each of the metallic walls with each layer of insulation material being of a different material than the dielectric material.

Claim 17 (Canceled).

18. (Original) An edge seal around the periphery of an integrated circuit device comprising:

a. a semiconductor substrate;

b. a layer of dielectric material over the semiconductor substrate, the layer of dielectric material comprising a low-k dielectric material;

c. a metallic wall in the layer of dielectric material; and

d. a wall of insulation material between the metallic wall and the periphery of the integrated circuit device wherein the insulation material and dielectric material are different materials.